REMARKS

The Office Action dated November 14, 2008 has been received and carefully noted. The above amendments to the claims, and the following remarks, are submitted as a full and complete response thereto.

Claims 26, 35, 41, 47, 48, and 50-54 have been amended to more particularly point out and distinctly claim the subject matter of the invention. No new matter has been added. Claims 26-37 and 41-56 are currently pending in the application and are respectfully submitted for consideration.

As a preliminary matter, Applicants wish to thank the Examiner for the courtesy extended in conducting a telephone interview on January 6, 2009.

The Office Action rejected claims 26-37, 41-47, and 49-56 under 35 U.S.C. §103(a) as being unpatentable over Kaniyar (U.S. Patent Pub. No. 2003/0187914) in view of Aviani (U.S. Patent No. 6,976,085). The Office Action took the position that Kaniyar discloses all of the elements of the claims, with the exception of informing the current connection state to respective processors comprising inserting data indicating the current connection state into a packet to be distributed. The Office Action then cited Aviani as allegedly curing this deficiency in Kaniyar. Applicants respectfully traverse this rejection because the combination of Kaniyar and Aviani does not disclose or suggest all of the limitations of the claims, as will be discussed in detail below.

Claim 26, upon which claims 27-37 are dependent, recites a method comprising obtaining a current connection state as well as a current load state of each of a plurality of

processors configured to perform communication in a packet switched connection. The method further includes selecting on a per received packet basis, by a load balancer configured to distribute load to said processors, a processor having a lowest load in such a manner that a respective next received packet is distributed to the processor irrespective of a specific connection to which this next received packet belongs. The method also includes maintaining information about the load state of each processor so that said selecting is performed by selecting one of said processors to serve and process a respective received packet based on the load state, and informing the current connection state to respective processors comprising inserting data indicating the current connection state into a packet to be distributed.

Claim 41, upon which claims 42-49 are dependent, recites an apparatus comprising selection circuitry configured to select, on a per received packet basis, one of a plurality of processors configured to perform communication in a packet switched connection on the basis of a stored load state of the selected processor in such a manner that a respective next received packet is distributed to the selected processor with a lowest load among said processors irrespective of a specific connection to which this next received packet belongs. The apparatus further includes connection state informing circuitry configured to inform the current connection state to respective processors by inserting data indicating the current connection state into a packet to be distributed.

Claim 50 recites a system comprising an obtaining unit configured to obtain a current connection state as well as a current load state of each of a plurality of processors

configured to perform communication in a packet switched connection. The system also includes a selector configured to select on a per received packet basis one of said processors, by a load balancer configured to distribute load to said processors in such a manner that a respective next received packet is distributed to the selected processor having a lowest load irrespective of a specific connection to which this next received packet belongs. The system further includes a maintenance unit configured to maintain information about the load state of each processor so that said selecting comprises selecting one of said processors to serve and process a respective received packet based on the load states, and an informing unit configured to inform the current connection state to respective processors comprising inserting data indicating the current connection state into a packet to be distributed.

Claim 51 recites a computer program embodied on a computer readable medium, the computer readable medium storing code comprising computer executable instructions configured to perform a method. The method includes obtaining a current connection state as well as a current load state of each of a plurality of processors configured to perform communication in a packet switched connection. The method further includes selecting on a per received packet basis, by a load balancer configured to distribute load to said processors, one of said processors in such a manner that a respective next received packet is distributed to said selected one of said processors having a lowest load irrespective of a specific connection to which a respective received packet belongs. The method also includes maintaining information about the load state of each processor so

that said selecting comprises selecting one of said processors to serve and process a respective received packet based on the load state, and informing the current connection state to respective processors comprising inserting data indicating the current connection state into a packet to be distributed.

Claim 52 recites a system comprising a plurality of processors configured to perform communication in a packet switched connection, and at least one load balancer configured to distribute the load to said processors. The load balancer is configured to obtain a stored current connection state and a current load state of each of said processors, maintain information about the load state of each of said processors, select a processor in such a manner that a respective next received packet is distributed to the processor having a lowest load irrespective of a specific connection to which a respective received packet belongs, and inform the current connection state to respective processors comprising inserting data indicating the current connection state into a packet to be distributed.

Claim 53 recites an apparatus comprising a load balancer. The load balancer is configured to obtain a current connection state and a current load state of each of a plurality of processors, maintain information about the load state of each of said processors, and select, on a per received packet basis, a processor having a lowest load in such a manner that a respective next received packet is distributed to the processor irrespective of a specific connection to which this next respective received packet belongs.

Claim 54, upon which claims 55 and 56 are dependent, recites an apparatus comprising maintaining means for maintaining a load state of each of multiple processors performing a packet switched communication connection. The apparatus also includes selecting means for selecting, on a per received packet basis, one of the processors on the basis of its load state in such a manner that a respective next received packet is distributed to a processor having a lowest load irrespective of a specific connection to which a respective received packet belongs. The apparatus further includes informing means for information the current connection state to respective processors by inserting data indicating the current connection state into a packet to be distributed.

Therefore, according to certain embodiments of the invention, processors are not dedicated to serve a specific connection or call. Rather, the load balancer can select any free processor on a per-packet basis irrespective of a specific connection to which a respective received packet belongs.

As will be discussed below, the combination of Kaniyar and Aviani fails to disclose or suggest all of the elements of the claims, and therefore fails to provide the advantages and features discussed above.

Kaniyar discloses a method for implementing symmetrical multiprocessing in a multiprocessor system and increasing performance of the multiprocessor system. More particularly, Kaniyar is directed to systematically partitioning I/O tasks for network connections across processors in the multiprocessor system so that each connection state

lives on a single processor for its lifetime. As a result, Kaniyar ensures that I/O tasks associated with a particular connection are processed by the same processor.

Aviani discloses a system that operates in a data communications device such as a switch or a router to provide a technique for inserting data into packets associated with a communications session between first and second computerized devices. The technique comprises receiving a first packet containing data being propagated from the first computerized device to the second computerized device in the communications session and inserting a first amount of extra data into the first packet to alter the size of the first packet, and then forwarding the first packet including the first amount of extra data to the second computerized device. By monitoring and adjusting sequence and acknowledgement information from with in the data communications device, data can be inserted into packets without disrupting connection state information maintained by and expected by each computerized device.

Applicants respectfully submit that the combination of Kaniyar and Aviani fails to disclose or suggest all of the elements of the present claims. For example, the combination of Kaniyar and Aviani does not disclose or suggest "selecting on a per received packet basis, by a load balancer configured to distribute load to said processors, a processor having a lowest load in such a manner that a respective next received packet is distributed to the processor irrespective of a specific connection to which this next received packet belongs," as recited in claim 26, and the similar limitations recited in claims 41 and 50-54. Thus, according to embodiments of the invention, a received data

packet is distributed to one of the processors irrespective of a specific connection to which the received packet belongs.

Kaniyar and Aviani, on the other hand, fail to disclose or suggest that a processor having a lowest load is selected, on a per received packet basis, in such a manner that a respective next received packet is distributed to the processor irrespective of a specific connection to which this next received packet belongs. The Office Action took the position that paragraph 0031 of Kaniyar discloses this limitation of the claims (see Office Action, page 3). Paragraph 0031 of Kaniyar discloses that the least busy processor in the system can be selected as a "scheduling processor." Therefore, this section of Kaniyar is directed to choosing a "scheduling processor," which is the processor that determines which processor in the system will process the packet. Accordingly, in Kaniyar, one of the processors is selected as the load balancing processor or "scheduling processor."

According to embodiments of the invention, on the other hand, a separate load balancing unit is provided to distribute the load. Furthermore, in embodiments of the invention, the load balancing unit selects a processor to process a received packet based on a lowest load and irrespective of a specific connection to which the received packet belongs. In contrast, according to Kaniyar, the "scheduling processor" selects the processor that has previously processed packets from the same network connection. In other words, Kaniyar teaches that packets received from the same network connection are scheduled for processing by the same processor, so that each connection state lives on a single processor for its lifetime (Kaniyar, paragraphs 0007, 0008, 0033). Thus, the goal

of Kaniyar is to systematically partition data streams for connections across processors to enable a connection state to live on a single processor for the lifetime of the connection which, in turn, enhances performance of the multiprocessor system (Kaniyar, paragraph 0033).

In view of the above, Applicants respectfully submit that Kaniyar fails to disclose or suggest "selecting on a per received packet basis... a processor having a lowest load in such a manner that a respective next received packet is distributed to the processor **irrespective of a specific connection to which this next received packet belongs**," as recited in claim 26, and similarly recited in claims 41 and 50-54. Rather, in direct opposition to what is recited in the present claims, Kaniyar discloses that packets received from the same network connection are always scheduled for processing by the same processor, so that each connection state lives on a single processor for its lifetime.

Furthermore, Aviani does not cure these deficiencies in Kaniyar. Aviani, as discussed above, merely discloses inserting connection information into data packets. Aviani, like Kaniyar, fails to disclose or suggest that a processor having a lowest load is selected, on a per received packet basis, in such a manner that a respective next received packet is distributed to the processor irrespective of a specific connection to which this next received packet belongs. Therefore, Applicants respectfully assert that the combination of Kaniyar and Aviani does not disclose or suggest "selecting on a per received packet basis, by a load balancer configured to distribute load to said processors, a processor having a lowest load in such a manner that a respective next received packet

is distributed to the processor irrespective of a specific connection to which this next received packet belongs," as recited in claim 26, and the similar limitations recited in claims 41 and 50-54. It is respectfully requested that the rejection of claims 26, 41, and 50-54 be withdrawn.

Claims 27-37, 42-49, 55, and 56 are dependent upon claims 26, 41, and 54, respectively. As such, claims 27-37, 42-49, 55, and 56 should be allowed for at least their dependence upon claims 26, 41, and 54, and for the specific limitations recited therein.

Claim 48 was rejected under 35 U.S.C. §103(a) as being unpatentable over Kaniyar (U.S. Patent Pub. No. 2003/0187914) in view of Aviani (U.S. Patent No. 6,976,085), and further in view of Reimer (U.S. Patent Pub. No. 2002/0059502). The Office Action took the position that Kaniyar and Aviani disclose all of the limitations of claim 48, with the exception of processors are comprised of multicore digital signal processing elements having a shared data storage for all cores, whereby said device comprises a first level of load balancing configured to select a digital signal processing means and a second level of load balancing configured to select a single core. The Office Action then cited Reimer as allegedly curing this deficiency in Kaniyar and Aviani. This rejection is respectfully traversed for at least the following reasons.

Kaniyar and Aviani are discussed above. Reimer discloses a multi-core digital signal processor having a shared program memory with conditional write protection. The digital signal processor includes a shared program memory, an emulation logic module,

and multiple processor cores each coupled to the shared program memory by corresponding instruction buses. The emulation logic module determines whether the processors are operating in a normal mode or an emulation mode. In the emulation mode, the emulation logic can alter the states of various processor hardware and the contents of various registers and memory. The instruction buses each include a read/write signal that, while their corresponding processor cores are in normal mode, is maintained in a read state. When the processor cores are in the emulation mode, the processor cores are allowed to determine the state of the instruction bus read/write signals. Each instruction bus read/write signal is generated by a logic gate that prevents the processor core from affecting the read/write signal value in normal mode, but allows the processor core to determine the read/write signal value in emulation mode.

Claim 48 is dependent upon claim 41 and inherits all of the limitations thereof. As discussed above, the combination of Kaniyar and Aviani fails to disclose or suggest all of the elements of claim 41. Furthermore, Reimer fails to cure the deficiencies in Kaniyar and Aviani, as Reimer also fails to disclose or suggest "selection circuitry configured to select, on a per received packet basis, one of a plurality of processors configured to perform communication in a packet switched connection on the basis of a stored load state of the selected processor in such a manner that a respective next received packet is distributed to the selected processor with a lowest load among said processors irrespective of a specific connection to which this next received packet belongs," as recited in claim 41. Thus, the combination of Kaniyar, Aviani and Reimer fails to

disclose or suggest all of the elements of claim 48. In addition, claim 48 should be allowed for at least its dependence upon claim 41, and for the specific limitations recited therein.

For at least the reasons discussed above, Applicants respectfully submit that the cited prior art fails to disclose or suggest all of the elements of the claimed invention. These distinctions are more than sufficient to render the claimed invention unanticipated and unobvious. It is therefore respectfully requested that all of claims 26-37 and 41-56 be allowed, and this application passed to issue.

If for any reason the Examiner determines that the application is not now in condition for allowance, it is respectfully requested that the Examiner contact, by telephone, the applicants' undersigned representative at the indicated telephone number to arrange for an interview to expedite the disposition of this application.

In the event this paper is not being timely filed, the applicants respectfully petition for an appropriate extension of time. Any fees for such an extension together with any additional fees may be charged to Counsel's Deposit Account 50-2222.

Respectfully submitted,

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